IN THE SPECIFICATION

Please amend the Title on page 1, line 1 as follows:

NONVOLATILE SEMICONDUCTOR MEMORY DEVICE HAVING PLURAL MEMORY CIRCUITS SELECTIVELY CONTROLLED BY A MASTER CHIP ENABLE TERMINAL OR AN INPUT COMMAND AND ~~OUPTTING~~ OUTPUTTING A PASS/FAIL RESULT

Please replace the paragraph beginning at page 7, line 35, with the following rewritten paragraph:

When the chip enable signal CE is deactivated, it is seldom that control is continued for each EEPROM circuit ~~is controlled continuously~~. Therefore, if the selection to each of the EEPROM circuits is released in connection therewith, the release of the selection can be easily controlled, and the subsequent control can be easily carried out.

Please replace the paragraph beginning at page 9, line 11, with the following rewritten paragraph:

FIG. 7 shows another preferred embodiment of a memory chip ld according to the present invention. In this preferred embodiment, an area selecting decoder 6 for selecting one of EEPROM circuits 2, which is to be written/erased, in response to an inputted command is provided in the memory chip ld between a common data bus 3 for the EEPROM circuits 2 and an external I/O terminal. This area selecting decoder 6 allows commands, addresses and data to be inputted to the I/O buffer of each of the EEPROM circuits 2 in time sequence. In this case, it is assumed that it is possible to optionally set the order in which the EEPROM circuits should be selected. Each of the EEPROM circuits 2 does not include a control circuit, as do the EEPROM circuits 2 in the non-limiting embodiments of Figures 1, 3, 5, and 6

~~controllers of command, address, and data~~. A single control circuit 7 for controlling writing or the like in the EEPROM circuits 2 is provided.